Laser-Induced Latchup Screening and Mitigation in CMOS Devices

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Abstract—**This paper describes application of the pulsed laser approach for identifying latch-up sensitive regions in CMOS circuitry. The utility of this approach for preliminary latchup screening of both COTS and space-qualified parts for applications in radiation environments is described. An application of hardening-by-design principles in which a space qualified CMOS product is modified, based on the pulsed laser results, to be latchup immune is presented in detail. The design modifications are described.**

Index Terms—latchup, micro-latchup, single-event effects, picosecond, laser, CMOS

I. INTRODUCTION

Single event latchup (SEL) occurs in CMOS integrated circuits (ICs) when the charge deposited by an ion passing through a sensitive node causes the IC to switch into a high current state. The sudden large current surge may physically damage the IC. In some cases the damage is so severe that the IC stops operating immediately after the SEL, whereas in other cases the damage does not affect the operation of the IC until much later. The latter case is termed "latent damage", because the initial damage gradually worsens with time until it becomes so severe that the IC stops operating. Obviously, in either case, engineers are wise to avoid using SEL-sensitive ICs for space applications.

The pulsed laser is a powerful tool for the interrogation of single-event upset (SEU) and single-event latchup (SEL) in microelectronic devices [1]-[7].

A primary advantage of laser-based techniques is the ability to locate and pinpoint sensitive regions of a device without the concomitant damage associated with accelerator techniques [3]. In this paper we describe the utility of the pulsed laser approach for identifying latchup sensitive regions in both COTS and space-qualified parts. This approach can be used for latchup screening of parts for applications in radiation environments. Additionally, the detailed spatial information provided by the laser analysis permits the intelligent and efficient application of hardening-by-design (HBD) principles through which latchup-sensitive parts can be modified to be SEL immune. Several case studies illustrating different aspects of the pulsed laser SEL approach are presented.

II. BACKGROUND

Early CMOS circuits contained very few connections to the power supply (V_{dd}) and to ground. As a result, the large electric current created by an SEL event was often sufficient to burn the gold wire that formed that connection. In later generations CMOS ICs were designed with many more connections to V_{dd} and ground, so that the current load was distributed. In this case physical damage began to occur instead in the metal interconnects of the IC itself: a sufficiently large current could melt, or even vaporize a metal interconnects, causing an IC malfunction. On the other hand, if the current only partially damages the metal interconnect, the IC may function properly once power is recycled. However, the latent damage associated with the SEL could eventually cause a premature functional failure of the IC so that the normal operating life of the IC could be greatly shortened.

Not all SELs cause physical damage. Some circuits are able to accommodate the increased current flow without any damage. Those circuits may be used in critical space applications, provided a method is used to detect and immediately cycle power to the IC. One approach is to use a current monitor that immediately sends a signal to cycle the power when the supply current exceeds a specified value that is just larger than the normal operating current.

Because there is no way *a priori* to identify which circuits will, and which will not be sensitive to latent damage, it is necessary to test representative ICs from the same date and lot codes for SEL. There are two

approaches for testing for SEL, each with its own advantages and limitations. One approach is to expose the IC to heavy ions at an accelerator and the other is to use pulsed laser light. A primary limitation associated with accelerator testing is the limited availability of time (and cost) to test the large number of parts that requires screening. Another is the lack of control over the details of the charge injection so that it is difficult to determine the location of the physical damage produced by the SEL (this limitation may be partially overcome by using an infrared camera to locate the "hot spot", which is assumed to be the location of the damage, although that correlation has not been verified in general). The pulsed laser overcomes these limitations because the laser pulse can be focused on a precise location and, if a SEL is produced at that location, the surrounding area can be easily scanned for damage.

In some cases the applicability of the pulsed laser technique is limited by metal coverage of the sensitive areas. For instance, the surfaces of FPGAs are almost completely covered with metal, preventing the optical radiation from reaching the sensitive areas of the silicon. Very dense memories, such as 256 Mbit SDRAMs, have so many metal layers over the individual memory cells that they can effectively block the laser light from reaching the underlying circuit layers. Fortunately, in this case, it has been demonstrated that SEL only occurs in the control circuitry of dense memories such as SRAMs and SDRAMs, and those areas are accessible to the laser.

Recently, a new method of laser-induced carrier generation that eliminates interference from the metal-ization layers has been introduced and demonstrated [10],[11],[12]. This method, which is based on the two-photon absorption (TPA) of high peak power femto-second laser pulses at sub-bandgap optical wavelengths, enables charge injection at any depth in the structure and permits charge injection through the wafer from the back side of the chip [11],[12]. The TPA approach represents an alternative method of injecting charge into modern devices that may have significant utility for latchup studies in the future.

III. EXPERIMENTAL

Heavy ion tests were performed the Tandem Van de Graaff at Brookhaven National Laboratory and at the Texas A&M particle accelerator. Measurements were performed with a range of ions at angles of incidence ranging from 0 to 60 degrees with incident ion LETs ranging from 2.8 MeV·cm^2/mg to 103 MeV·cm^2/mg. The devices were irradiated typically to a particle fluence of greater than 1×10^7 particles/cm^2, or until latchup occurred.

The laser-induced SEL measurements of this study were performed at the Naval Research Laboratory single-event effects facility with nominally 1 ps duration optical pulses centered at 590 nm (2.1 eV) with an optical 1/e penetration depth in silicon of approximately 1.8 µm [4]. The experimental setup is illustrated in Fig.

1. The laser pulse repetition rate can be varied between single shot and 1 MHz; the experiments reported here were performed at a pulse repetition rate of 1 KHz. The optical pulses are focused onto the device under test (DUT) with a 100x microscope objective, resulting in a Gaussian spot size of 1.2 µm at the surface of the DUT. The DUT is mounted on a motorized xyz stage with 0.1 µm resolution, and the laser-induced SEL thresholds are determined by optimizing the xy position and focus (z) to obtain the minimum laser pulse energy able to induce latchup. The pulse energy is monitored with a calibrated large-area photodiode, and the incident pulse energy is converted into deposited charge by correcting for reflection losses and assuming that each photon gives rise to a single electron-hole pair. Incident pulse energies can be converted to an effective LET using the empirical relationship established previously [2],[3].
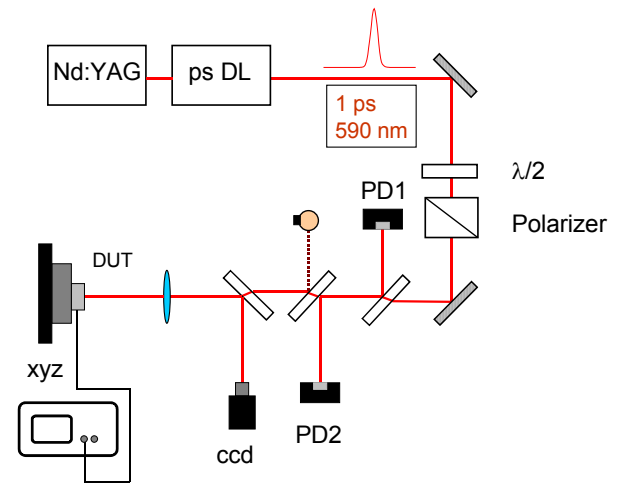

Fig. 1. Experimental configuration used for the laser SEL experiment. Nd:YAG: modelocked neodymium YAG laser; λ/2: half wave plate; PD1, PD2: large-area photodiodes; xyz: xyz translation stage; ccd: silicon ccd camera; DUT: device under test.

IV. LATCHUP SCREENING OF COTS PARTS

The currents produced by ionization-induced latchup in a microelectronic device can lead to catastrophic failure of that device. Consequently, devices to be used in satellite systems, particularly CMOS devices, must be screened for latchup. Devices that are sensitive to latchup typically are eliminated from consideration in space systems.

The latchup evaluation of COTS parts may be performed with a pulsed picosecond laser. Application of the pulsed laser methodology to the latchup screening of COTS parts has become a common procedure for minimizing the amount of heavy ion testing required to screen parts for application in radiation environments, although much of that work remains unpublished. In this application the pulsed laser irradiation is used simply to determine whether, or not, a part will latchup following an ionization event. In many cases the pulsed laser results can be correlated with heavy-ion SEL thresholds

[2],[3], but this correlation often is not required for screening applications. In what follows we present a series of examples illustrating how the pulsed laser is used to investigate and characterize different aspects of latchup in a number of different COTS devices types.

A. RDC-19220 Resolver-to-Digital Converter

Figure 2 shows a photomicrograph of an RDC-19220 resolver-to-digital converter (RDC) manufactured by ILC Data Device Corporation [8]. In this series of tests two RDCs were evaluated for potential use in a NASA space mission. As is evident, for the RDC-19220, SEL is observed over a significant fraction of the surface area of the chip. Additionally, the laser induced latch-up threshold was measured to correspond to 1.4 pC of deposited charge (2.8 pJ pulse energy). This value is indicative of a high level of sensitivity. Using the previously determined empirical correlation factor that has been found appropriate for SEU and SEL in many CMOS parts [2],[3], this measurement corresponds to a threshold LET of approximately 8 MeV·cm^2/mg. Based on these results, the RDC-19220 was eliminated from consideration for future NASA missions.
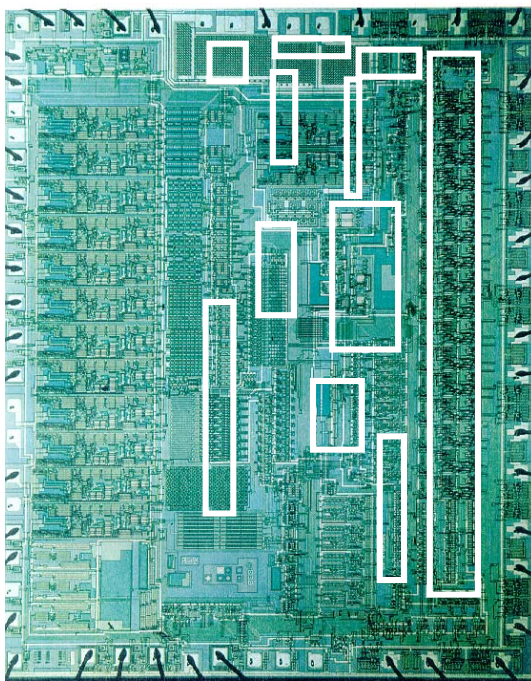

Figure 2. Photomicrograph of an RDC-19220 resolver-to-digital converter illustrating the latchup-sensitive areas identified by the pulsed laser [8].

The second RDC investigated in that study (Analog Devices, Inc., AD2S80) was found by the laser to be SEL free, a result that was confirmed in subsequent HI testing.

It is important to note that the absence of laser-induced latchup in a part does not unequivocally eliminate the possibility of latchup in a radiation environment. Interference by device metallization can shield latchup sensitive regions of a device, and

additional ion testing may be desirable for flight validation. Intelligent decisions in this regard can be made based on the metal coverage of the part. That said, to date we have not tested a single part that latched under heavy ion irradiation and failed to latch with the 590 nm pulsed laser.

B. LXA0387 512 Kbit SRAM

Pulsed laser SEL testing was performed on bulk 512 Kbit SRAMs (LSI logic LXA0387; 0.18 μm CMOS; 1.8 V). This test was performed for several reasons: to identify the SEL sensitive regions of the chip; to determine the physical cross section of this sensitive region; and to determine whether the latch-up events are damaging or not.

The memory array is organized as 64K 8 bit words; static and dynamic tests were performed with four different test patterns: all 1's; all 0's, checkerboard; and reverse checkerboard. The power supply currents of the device were monitored to detect the occurance of latchup or other anomalous conditions. In the case of SEL the detection threshold was set to 1 mA for the memory core power supply and to 20 mA for the I/O and periphery power supplies. If these values were exceeded the power supply was shut down. The device was operated at 1 MHz at the nominal power supply voltage of 1.8 V.

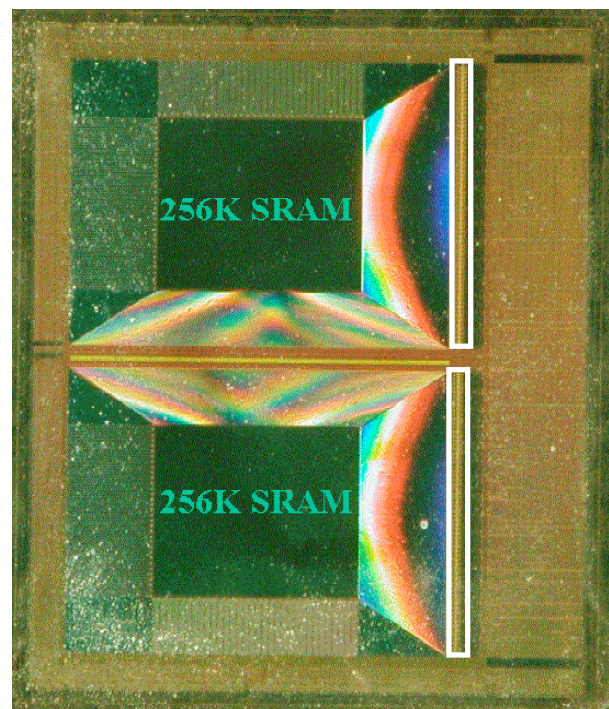Fig. 3. Photomicrograph of a LSI logic LXA0387 512 Kbit SRAM illustrating the latchup-sensitive areas identified by the pulsed laser (outlined in white).

In heavy-ion tests, latchup was observed for ion LETs of greater than 29 MeV·cm^2/mg. Fig. 3 shows a photomicrograph of an LXA0387 indicating the latchup-sensitive areas identified by the pulsed laser. The SEL sensitive regions of this part are limited to the control

circuitry and, as is evident, constitute a relatively small fraction of the total chip area. In making this determination, to assure that all sensitive areas of the chip were identified, the laser pulse energy was adjusted to deposit a significantly higher quantity of charge than could be generated by any ion. In this case, the laser pulse energy was greater than 200 pJ, which corresponds to an effective LET of significantly greater than 100 MeV·cm^2/mg.

An additional major concern for the design engineer is whether the latchup events are destructive or non-destructive. In this case the maximum SEL current was observed to be 160 mA, and full device performace could be recovered by cycling the power. Therefore, at least from this measure, the latchups in the LXA0387 are considered to be non-damaging. This does not address the issue of latent damage, which is discussed in more detail in the following.

C. Latent Damage: 256 MKbit SDRAM

In addition to the manifestations of obviously destructive latchup events, an additional very significant concern for the design engineer is the possibility of latent damage. Latent damage caused by latchup may, or may not, be observable. It has been suggested that, if the current density in a metal interconnect approaches 1 x 10^7 A/cm^2, the resulting damage is so severe that it is visibile with an optical microscope [1]. Current densitites in the range of 1 x 10^6 A/cm^2 present more of a problem because they are more likely to produce microscopic damage that cannot be detected optically [13]. Evidence of physical damage may be obtained through the use of an electron microscope, but that technique is not generally available and is more suited to a research project than to routine evaluations of latchup.

We note that a single part may exhibit multiple latchup modes, some of which may be non-destructive and some of which may have latent damage. Therefore, when testing at an accelerator with a broad beam of heavy ions, all latchup modes will be generated, provided a sufficiently high fluence is used (it is generally agreed that a fluence of 1 x 10^7 particles/cm^2 is sufficient to induce latchup in all possible locations). The different latchup modes may sometimes be distinguish by their current signatures, that is, latchups with large currents that rise rapidly are more likely to produce latent damage than latchups with small currents.

An illustration of how to perform latchup testing that includes the possibility of latent damage is the testing performed on the Elpida 256 Mbit SDRAM. Heavy-ion testing showed that the part had a latchup threshold between 54 MeV·cm^2/mg and 64 MeV·cm^2/mg. Program managers are loath to permit the use of parts that have latchup thresholds below 100 MeV·cm^2/mg unless it can be demonstrated that there is no immediate damage as well as no latent damage.

To comply with these requirements, a number of the SDRAMs were exposed to heavy ions with sufficient LETs to produce latchup. Each time the power was cycled and the part operated as expected. Optical inspection failed to reveal any indication of physical damage that could impact the lifetime of the part. In order to prove to the program manager that the parts presented no danger to the mission, accelerated life testing (the part was kept at 125 C for 100 days) was performed on all the parts that had undergone multiple latchups. Those tests gave no evidence of diminished lifetime, suggeseting that latchup caused neither immediate nor latent damage in the parts. As a result, those parts will be flown in future NASA missions.

The pulsed laser was also used to induce latchup. The main goal was to determine whether repeatedly triggering latchup in the same location could eventually cause observable damage that could later lead to diminished lifetime. No such damage could be induced by the pulsed laser. We should point out that no lifetime testing was performed on the part exposed to the pulsed laser.

V. LATCHUP EVALUATION AND MITIGATION THROUGH LAYOUT REDESIGN

A National Semiconductor DS90C031 LVDS (low voltage differential signaling) quad differential line driver was thought to have sufficient radiation tolerance to be designed into the recent global positioning system (GPS) upgrade program (the DS90C031 is a fully space qualified manufacturers list (QMLV) part). Subsequent heavy ion testing, however, revealed an unanticipated latchup susceptibility that rendered the part unacceptable for GPS use, with a delay in the mission launch date (and the associated increase in mission cost) being a distinct possibility. Evaluation of the latchup susceptibility of the part with the pulsed laser approach revealed, however, that latchup was limited to a single, localized region in the circuit, suggesting the possibility that relatively minor modifications of the layout could eliminate the problem. Through close collaboration of the various parties involved (National Semiconductor, Boeing, NASA, Sandia), the part was redesigned, fabricated, and retested in a timely fashion, and the mission was launched on schedule.

A. Preliminary Ion Tests

Two rounds of heavy ion tests were performed on a total of 6 parts. Latchup was observed in four of the six parts, with latchup observed in one part at the lowest LET tested (37 MeV·cm^2/mg).

B. Laser Latchup Interrogation

Scanning the focused laser pulse across the surface of the device resulted in latchup in only a single, localized region, even for the highest values of deposited charge. This region is indicated as "B" in Fig. 4 and can be described as a parasitic PNPN SCR with a latchup path involving the PMOS source at V$_{dd}$, its associated N-well, the P$^-$ substrate, and the grounded end ("A") of the N$^+$ resistor diffusion ("C" in Fig. 4). Based on these results additional areas having potential latchup structures were

identified. These included additional PMOS source-to-resistor paths (path "1" in Fig. 3), and more traditional PMOS source to NMOS source paths, indicated by path "2" in Fig. 3.
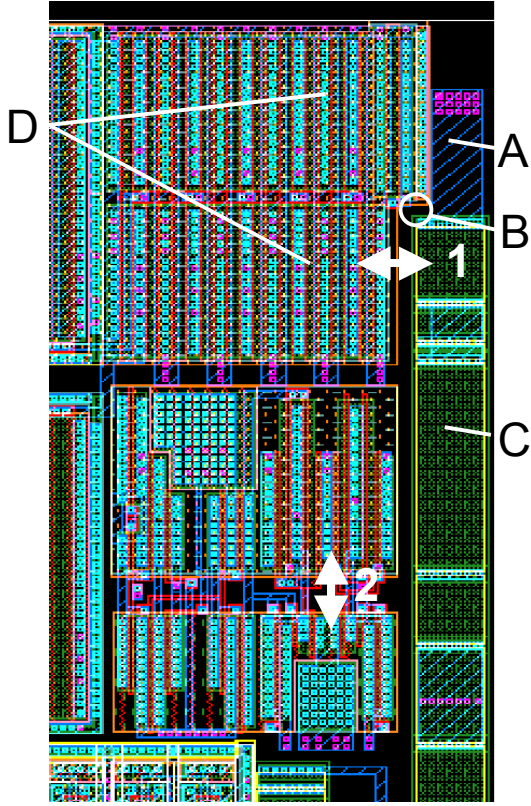

Figure 4. Original layout of National Semiconductor DS90C031 LVDS quad differential line driver. "A" is ground, the area "B" was identified by the laser as being latchup sensitive; structure "C" is a resistor; and structure "D" is a (large) drive transistor. Additional areas with potential latchup pathways are indicated by "1" and "2".

C. Redesign Using HBD Methodology

Several design modifications were made to reduce the sensitivity of this part to latchup. The modified layout is shown in Fig. 5. The latchup-sensitive region identified by the laser represents the closest spacing of the PMOS driver transistor and the N+ resistor diffusion. The distance between the N-resistor and N-well was increased in order to decrease the lateral NPN bipolar gain. The width of the P-well along th PMOS source stripe was increased in order to decrease resistance between the emitter and base of the parasitic PNP. Finally, P$^+$ and N$^+$ guard stripes were added in the P-substrate and N-well regions, as space allowed, to clamp voltage gradients.

The specific latchup region identified by the laser interrogation had sufficient room for the insertion of both P$^+$ and N$^+$ guard stripes. These are identified in Fig. 5, and were extended along the entire length of the resistor. A single (horizontal) P$^+$ guard stripe was inserted between the NMOS and PMOS blocks (*cf.,* Fig. 5). Several separate N$^+$ contact points were inserted along

the edge of the N-well. As an added precaution, two additional potential latchup regions not shown in Fig. 4 were modified in a similar manner.
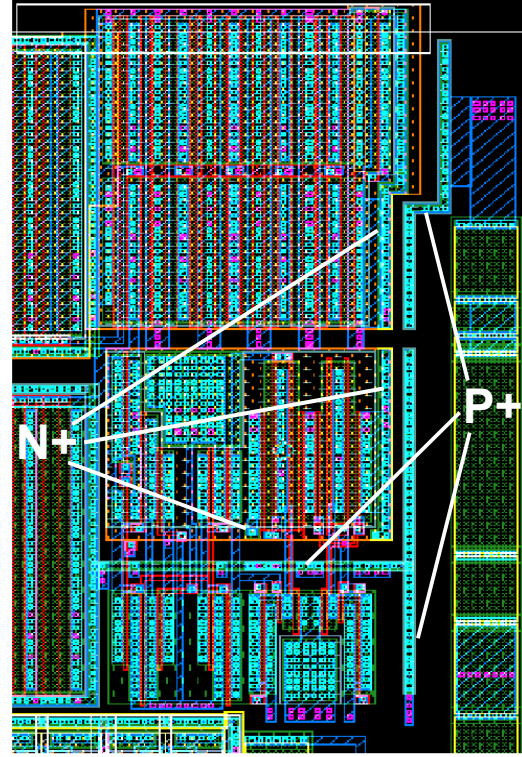

Figure 5. Layout of National Semiconductor DS90C031 LVDS quad differential line driver following design modification for latchup hardening of areas indicated in Fig. 3. Locations of the P$^+$ and N$^+$ guard stripes are indicated.

Even though these added features increased the area of the circuit, the die bond pads remained in their original positions with the same pin-out and package footprint as the commercial part was maintained.

D. Final Ion Tests

Heavy ion tests were performed on three of the redesigned parts (no laser tests were performed). All tests were carried out at a worst case bias of 5.5 V, with LETs ranging from 38 MeV·cm^2/mg to 103 MeV·cm^2/mg, and a fluence in excess of of 4×10^7 ions/cm^2 for each run. No latchup was observed.

As a consequence of the close collaboration and cooperation between several different industrial and government entities, the problem was identified and the redesign achieved in a timely fashion, and the mission was carried out on schedule.

It should be noted that the heavy-ion tests described in this section were performed before the role of ion track length was fully appreciated, and do not meet the presently accepted criteria for latchup screening. Recently, the importance of testing with ion ranges on the order of 100 um has been acknowledged (especially when overlayers are considered) [9]. The use of ions with shorter ranges can lead to erroneously low cross section values, and should be avoided [9].

VI. EVALUATION OF MICRO-LATCHUP IN ASIC TEST CHIP

Pulsed laser testing was performed on an LSI Logic LXA0381 ASIC to investigate the observation of high current anomalies (HCAs) observed in heavy ion testing.

The logic test chip contains 64, 64-bit ALUs, and is designed with full scan methodology. There are 4 scan chains with a length of 3072 flip-flops each. This design was synthesized to operate at a maximum speed of 20 MHz. The I/O buffers consist of 3 voltage types 1.8V, 2.5V, and 3.3V. A picture of the logic test chip is shown in Fig. 6. The logic test chip is packaged in a 313 pin plastic EPBGA package.

In heavy-ion testing for LETs higher than 2.8 MeV·cm^2/mg large bursts of errors are observed, and the device stops functioning. Analysis of the 1.8V power supply current files showed high current anomalies involving successive current jumps of 10 to 60 mA from its nominal value. As soon as the first HCA occurs the device stops functioning properly; a power cycle is necessary to recover functionality. Even after the device ceases to function, however, the current files indicate a continual increase in the current until the power is cycled. The signature of this effect is consistent with a series of micro-latchups induced by individual ions. A micro-latchup is a latch-up initiated by a single heavy ion (or laser pulse) in which the current is limited by the device internal circuitry. Since the current is limited, the micro latch-up is not destructive, but the effect on device functionality can be significant. The pulsed laser was used to investigate this effect in the LSI logic test chip.

Fig. 6 shows a photomicrograph of the LSI logic test chip. The pulsed laser was used in single-shot mode to inject charge at the locations indicated in the order shown. The results of one series of tests are shown in Fig. 7. The first laser pulse (at time τ_1) results in a current increase of 50 mA, from the nominal operating current (16 mA) to 60 mA. The second laser pulse at location 2 (at time τ_2) gives rise to a smaller increase of 15 mA, with the third pulse (at τ_3) resulting in an increase to 106 mA.

Additional measurements were performed to gain insight into the nature of the individual micro-latches. In particular, it was found that once a micro-latch is initiated at a given location, successive laser pulses at that location lead to no further increase in the current. Charge injection at a different location leads to the effects illustrated in the data of Fig. 7.

The practical ramification of these results for the satellite designer is the critical nature of choosing the proper set point for power cycling. This is because a micro-latch, however small, renders the device (or part of it) inoperable. If the current limit is set too high, a single such event could result in significant dead time for the part, a result that may be unacceptable for the mission.
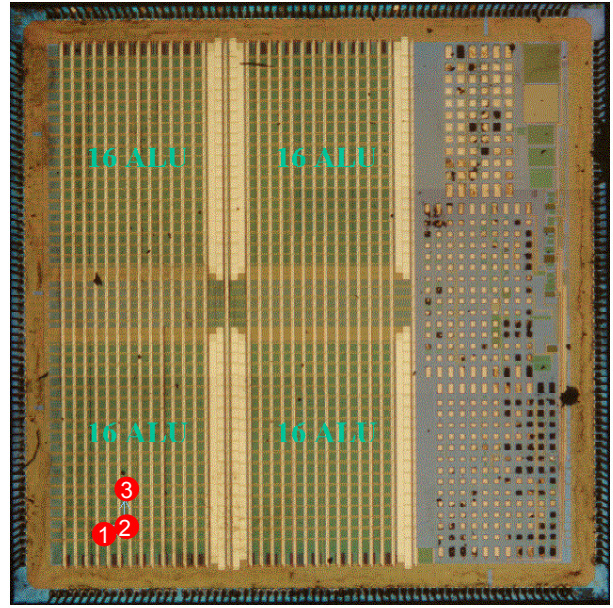

Fig. 6. Photomicrograph of a LSI logic ASIC test chip. The locations and sequence of the laser-induced micro-latch events illustrated in Fig. 7 are indicated.
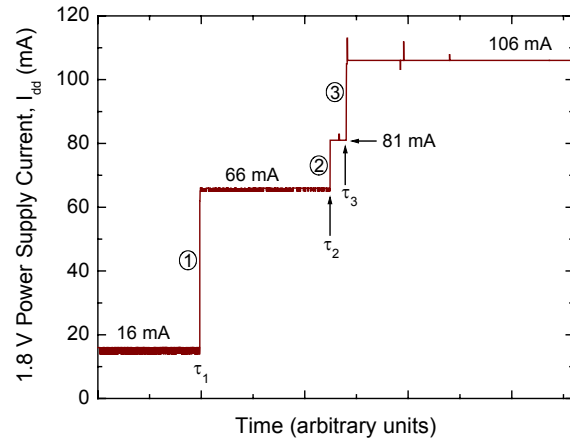

Fig. 7. Representative data illustrating the current evolution for the 1.8 V power supply for successive laser pulses incident on the three locations indicated in Fig. 6.

VI. DISCUSSION AND CONCLUSIONS

The results presented illustrate the utility of the pulsed laser approach for latchup interrogation, screening, and mitigation for COTS and space-qualified CMOS devices. Latchup screening of CMOS parts for space missions using the pulsed laser is becoming more common, but still is not widespread. Implementation of laser interrogation as the initial step in the screening process can result in significant program savings in terms of both personnel time and accelerator costs. Additionally, if modification of a latchup sensitive device is possible, or required by specific mission constraints, then the detailed spatial information provided by the laser interrogation permits this modification to be implemented in the most efficient and cost effective manner.

All of the examples of this study utilize the 590 nm output of a Rhodamine dye laser. While very effective for each of the examples presented, this choice of laser wavelength results in effectively all of the charge being deposited in the top 5 μm of the silicon. This may not be the most appropriate choice for general (future) applications.

Recently, the mechanisms of laser-induced latchup have been investigated for well-characterized epitaxial device structures using optical pulses having different charge-deposition profiles [6]. Those results provide specific insights into the roles of the vertical PNP and lateral NPN parasitic transistors that are responsible for the latchup process for both heavy-ion and pulsed laser irradiation. It was found that, for the devices studied, threshold measurements with more deeply penetrating 815 nm optical pulses exhibit good agreement with heavy ion threshold measurements, and favor triggering either the vertical PNP transistor or a combination of both the vertical and lateral transistors. In contrast, at threshold, the visible (600 nm) pulses preferentially trigger the lateral NPN transistor, and exhibit a dependence of the threshold on the well-to-diffusion separation that is not observed in the heavy-ion measurements [6].

While the generality of those results to other device structures has not been verified (and it may be difficult to do so [6]), the use of more deeply penetrating optical pulses for laser-induce latchup screening is reasonable. We note, however, that latchup screeing applications, such as those described here, do not typically utilize near-threshold laser pulse energies, and the quantitative determination of the latchup threshold is not generally a concern. In this light, the specific relevance of the results of [6] to the present work is not clear, and will require further work before any firm conclusions can be made. We reiterate the observation that we are not aware of a single device that is susceptible to SEL under heavy ion irradiation that has failed to latch up with the 590 nm pulsed laser.

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